Curriculum Vitae of Pierpaolo Palestri

Pierpaolo Palestri was born in 1973. In 1998, he received the Laurea degree in Electronic Engineering from the University of Bologna, Italy, with a thesis on impact ionization in bipolar transistors. From 1998 to 2000, he received a research grant from the University of Udine, Italy, where he worked on the simulation and optimization of bipolar transistors and on the analysis of hot electron phenomena in MOS devices and non-volatile memories. From July 2000 to October 2001 he was a Post-Doctoral Member of Technical Staff at Bell Labs (Lucent Technology, Murray Hill, New Jersey), working on the simulation and experimental characterization of silicon-germanium bipolars. In November 2001, he became Assistant Professor at the University of Udine, where he then finished his PhD in 2003. Since November 2005, he has been Associate Professor of Electronics at the University of Udine.

Scientific activity

The scientific activity of P.Palestri has been mainly focused on the development of sophisticated modeling tools for electron devices. He has been involved (in many cases as the principal investigator) in the development of models to simulate many devices such as SiGe bipolars, nanoscale MOSFETs and non-volatile-memories with different architectures. Concerning bipolars, the focus has been on the current-voltage and RF characteristics, but efforts have been devoted also to the modeling of device breakdown, thermal resistance and device reliability. Concerning nanoscale MOSFETs, sophisticated Monte Carlo models have been developed for the analysis of the channel mobility and of the current drive in the presence of the main technology boosters (strain and high-k dielectrics) and for innovative device architectures (SOI, finFET, tunnel-FET) as well as for alternative channel materials (SiGe, III-V, graphene). Models for non-volatile memories have been developed to study the injection efficiency, but also phenomena such as read and write disturbs, retention and cell reliability. In many cases the modeling activities have been complemented by extensive experimental characterization on samples made available by many companies and Universities in the framework of European projects/networks or specific contracts. Commercial TCAD tools, after suitable customization/calibration, have been used to optimize nano-biosensors (for detection of molecules) and particle detectors (for high energy physics experiments).

These activities on electron device modeling have been carried out in collaboration with companies such as Philips Eindhoven and NXP Leuven (optimization of silicon bipolars, modeling of non-volatile memories), TSMC Taiwan/ TSMC Europe/ NXP Leuven (modeling of finFET devices and alternative channel materials), STMicroelectroncis Crolles (modeling of non-volatile memories, MOSFET reliability).

In the framework of a long standing collaboration between the University of Udine and Infineon Technologies (the design center in Villach, Austria, is about 1h drive from Udine) P.Palestri has been involved in the modeling and design of basic building block for RF systems (phase-locked-loops, low-noise-amplifiers, voltage-controlled-oscillators, frequency dividers) and, more recently, transmitters for high-speed serial links. Ongoing activities on Radio-Frequency Identification (RFID) in cooperation with medium and small-size companies in the Friuli-Venezia-Giulia region concern hardware and software development in the HF and UHF range.

Pierpaolo Palestri regularly acts as a reviewer for IEEE Electron Device Letters, IEEE Transactions on Electron Devices, IEEE Transactions on Circuits and Systems II, Solid State Electronics, Semiconductor Science and Technology. In 2008 and 2009, he served as a member of the “Modeling and Simulation” committee of the International Electron Device Meeting. He has been one of the organizer of the ULIS conferences in 2003 and 2008, when the conference has been held in Udine, and he has been one of the Guest Editors of the Special Issue of Solid State Electronics (April 2009) devoted to such conference. Since March 2012, he is in the program committee of the ULIS conference.

Pierpaolo Palestri is a senior member of the IEEE.

Involvement in European and national projects

Pierpaolo Palestri is, or has been, the scientific coordinator for the University of Udine of the following projects:

- Network of Excellence "Nanofunction" (FP7/2007-2013 n.257375), European NoE in which the University of Udine is involved in the simulation of nano-biosensors (~ 40Keuro) ;
- Cooperlink (funded by the Italian MIUR) "Exchange of PhD students and courses in electronics" (CII11AVUBF) between Univ. Udine and KTH (Royal Institute of Technology) Stockholm (~ 25Keuro);
- FIRB Futuro in Ricerca 2010 “Dispositivi e circuiti di nuova concezione per un'elettronica a basso consumo” (Novel device and circuit concepts for energy-efficient electronics), project funded by the Italian MIUR and devoted to the modeling of advanced electron devices, such as tunnel-FETs, intended for low energy operation (~ 160Keuro);
- e^2switch (Energy Efficient Tunnel FET Switches and Circuits, 619509), E.U. project on low energy switches, in which the University of Udine performs device and mixed device-circuit simulations of tunnel-FETs (~ 150Keuro).

In 2010-2012, Pierpaolo Palestri has been the scientific responsible for the contract with the paper mill "Gruppo Cordenons" (Pordenone, Italy) concerning the embedding of radio-frequency identifiers (RFID) into the paper (~ 10Keuro).

Besides, Pierpaolo Palestri has been involved in the proposal preparation, in the implementation and in the reporting of the following EU projects:

- EUROSOI (IST-1-506653), network on silicon-on-insulator technologies,
- PULLNANO (IST-026828), project devoted to the development of MOSFETs for the 32nm technology node,
- SINANO (IST-506844), network on silicon nanodevices (fabrication, modeling, characterization),
- NANOSIL (IST-216171) continuation of SINANO,
- STEEPER (IST-257267), project devoted to the development of low-energy switches / tunnel-FETs,
- Guardian Angels (IST-285406), flagship on zero energy devices/circuits/systems,
- GRAND (IST-215752), project devoted to the fabrication, modeling and characterization of graphene devices,
- MODERN (IST -216537), Eniac-JTI project devoted to variability in nanodevices,
- GOSSAMER (IST-214431), project devoted to fabrication, modeling and characterization of non-volatile memories with trapping layers,
- GRADE (IST-317839), project devoted to fabrication, modeling and characterization of graphene devices for RF applications,
- III-V-MOS (Technology CAD for III-V Semiconductor-based MOSFETs, 619326) project devoted to the modeling of III-V nMOSFETs, coordinated by the nanoelectronics group of the University of Udine.
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It has been also involved in the proposal preparation, in the implementation and in the reporting of the following Italian MIUR projects:

- PRIN 2000: "Permeable gate CMOS circuits: are they feasible ?",
- FIRB 2001: "Miniaturized systems for electronics and photonics" (RBNE012N3X),
- PRIN 2002: "Sub 0.1 micron Bulk and SOI CMOS Technologies for High Performance and Low Power
- Application",
- PRIN 2004: "Innovative Architectures and Models for nanoMOSFETs",
- MIUR Interlink 2004-2006: "Internazionalizzazione del Dottorato di Ricerca in Ingegneria Industriale e dell'Informazione",
- FIRB 2006: "Innovative technologies for the development of non volatile memories with high density" (RBIP06YSJJ),
- PRIN 2006: "Conventional (bulk) versus emerging nanoscale CMOS technologies: a comparative evaluation from the device to the system level",

- PRIN 2008: "Modeling and simulations of graphene transistors for digital applications with high performance and low power dissipation (GRANFET)".

Teaching activities

Courses at the University of Udine

- "Elettronica per le telecomunicazioni I" (Master level, 6 CFU), now "Sistemi elettronici per le alte frequenze", RF electronics at the system level, academic years from 2004/05 to 2013/14;
- "Elettronica per le telecomunicazioni II" (Master level, 6 CFU), now "Circuiti elettronici per le alte frequenze", RF electronics at the circuit level, academic years 2002/03, 2003/04, 2008/09, 2009/10 and 2010/11;
- "Strumentazione e misure elettroniche" (Master level, 6 CFU), electronic instrumentation in the frequency domain (spectrum analyzer, network analyzer), academic years from 2005/06 to 2009/10
- "Fondamenti di elettronica digitale" (Bachelor level, 6CFU), basic of digital electronics, academic years from 2011/12 to 2013/14

Tutoring

Pierpaolo Palestri has been the tutor of five PhD students at the University of Udine since 2005:

- D.Ponton, design of RF circuit building blocks using non-conventional technologies (finFETs, ultra-scaled MOSFETs with high-k),
- P.Toniutti, modeling of MOSFETs with high-k dielectrics,
- A.Cristofoli, modeling and design of high-speed serial links,
- P.Osgnach, development of efficient numerical simulation models for nanodevices,
- E.Caruso, modeling of nanoscale transistors with III-V semiconductor channels.

He also tutored approximately 20 Master theses and 15 Bachelor theses.
Pierpaolo Palestri is the coordinator of the ERASMUS agreement between the University of Udine and KTH (Royal Institute of Technology) Stockholm, Sweden.

Summary of the bibliometric data

Pierpaolo Palestri published 81 papers on international journals with peer-review, more than 100 contributions in international conferences with peer-review, 7 chapters in edited books and one book for Cambridge University press.

According to Harzing's "Publish or Perish", those publications have (March 2014):

- 1603 citations
- h-index=22
- contemporary h-index=17

The three publications selected by Pierpaolo Palestri for the Italian VQR as well as other six publications with Pierpaolo Palestri as coauthor submitted by the colleagues F.Driussi, D.Esseni and L. Selmi have been all rated "excellent".